

# **INFORMATION DISCLOSURE STATEMENT BY APPLICANT**

Application Number 10/531,009  
 Filing Date 06/10/2005  
 First Named Inventor BURNS, Geoffrey  
 Art Unit Unknown 2112  
 Examiner Name Unknown Vincent Fong  
 Attorney Docket Number US02 0543 US

## **U.S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Document Number No.-Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns Lines, Where Relevant Passages or Relevant Figures Appear
VF	1	US- US 2003/0065904	04-03-2003	GEOFFREY BURNS ET AL	
VF	2	US- US 5 974 537	10-26-1999	VIJAY KRISHNA MEHRA	
VF	3	US- 60/432971		G.BURNS ET AL	

## **FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Document Number (ctry <sup>3</sup> -no. <sup>4</sup> -kind <sup>5</sup> , if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited document	Pages, Columns Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>

## **NON-PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in capital letters), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>6</sup>
VF	1	MIYAMORI T ET AL: "REMARC: RECONFIGURABLE MULTIMEDIA ARRAY COPROCESSOR"; IEICE TRANSACTIONS ON INFORMATION AND SYSTEMS, INSTITUTE OF ELECTRONICS INFORMATION AND COMM. ENG.; TOKYO, JP; Vol. E82-D, no. 2; February 1999 (1999-02); pages 389-397	
VF	2	CUCCHIARA R ET AL: "RECONFIGURING THE BOUNDARIES OF A MESH-CONNECTED ARRAY OF PROCESSORS . . ."; MICROPROCESSORS AND MICROSYSTEM, IPC BUSINESS PRESS LTD; LONGDON, GB; Vol. 17, no. 2; January 1993 (1993-01); pages 67-73	
VF	3	BARAT F ET AL INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS: "RECONFIGURABLE INSTRUCTION SET PROCESSORS: AN IMPLEMENTATION . . ."; CONFERENCE RECORD OF THE 35 <sup>TH</sup> ASILOMAR CONFERENCE ON SIGNALS, SYSTEMS, & COMPUTERS; PACIFIC GROOVE, CA; NOV 4-7, 2001; ASILOMAR CONFERENCE ON SIGNALS, SYSTEMS AND COMPUTERS, NEW YORK; Vol. 1 of 2 CONF. 35; 4 NOV. 2001; pages 481-485	
VF	4	CALLAHAN T J ET AL: "THE GARP ARCHITECTURE AND C COMPILER"; COMPUTER, IEEE COMPUTER SOCIETY; LONG BEACH, CA, US; Vol. 33, No. 4, April 2000 (2000-04); pages 62-69	

Examiner Signature	/Vincent Fong/ (12/15/2006)	Date Considered	12/15/2006
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\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Unique citation designation number. <sup>2</sup> See attached Kinds of U.S. Patent Documents. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

<b>INFORMATION DISCLOSURE STATEMENT TRANSMITTAL</b>  To Commissioner For Patents Enclosed herewith is a Form PTO-1449, any required copies of documents listed thereon, and any concise explanation of their relevance is indicated below per 37 CFR 1.97.	Application Number	10538369
	Filing Date	
	First Named Inventor	Geoffrey F. Burns
	Group Art Unit	2112
	Examiner Name	Vincent Fong
	Atty. Docket Number	US02 0543 US

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		US-			
		US-			

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VF	1	MIYAMORI T ET AL: "Remarc: Reconfigurable multimedia array coprocessor", IEICE TRANSACTIONS ON INFORMATION AND SYSTEMS, February 1999, Vol. E82-D, No. 2, pages 389-397, Institute of Electronics Information and Comm. Eng. TOKYO, JP				
VF	2	CUCCHIARA R. ET AL: "Reconfiguring the boundaries of a mesh-connected array of processors with run-time programmable logic", JOURNAL OF MICROPROCESSORS AND MICROSYSTEMS, January 1993, Vol. 17, No. 2, pages 67-73, IPC Business Press Ltd., LONDON, GREAT BRITAIN.				
VF	3	BARAT F ET AL.: "Reconfigurable instruction set processors: an implementation platform for interactive multimedia applications" CONFERENCE RECORD OF THE 35 <sup>TH</sup> ASILOMAR CONFERENCE ON SIGNALS, SYSTEMS & COMPUTERS. Pacific Grove, CA Nov. 4-7, 2001, Asilomar Conference on Signals, Systems, & Computers, NEW YORK, NY. Vol. 1 of 2, Conf. 35, 11/4/2001, pages 481-485				
	4	SINGH H ET AL: "MorphoSys: a reconfigurable architecture for multimedia application s" INTEGRATED CIRCUIT DESIGN, 1998. PROCEEDINGS. XI BRAZILIAN SYMPOSIUM ON RIO DE JANEIRO, BRAZIL, 9/30 - 10/3, 1998, LOS ALAMITOS, CA, USA, Pages 134-139.				

Examiner Signature	/Vincent Fong/ (12/15/2006)	Date Considered	12/15/2006
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